Reg No.: $\qquad$ Name: $\qquad$

## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY THIRD SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

## Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN
Max. Marks: 100
Duration: 3 Hours

## PART A

Answer all questions, each carries $\mathbf{3}$ marks
1 Perform the following operations:
i) $(\mathrm{E} 39)_{16}+(3 \mathrm{~F} 9)_{16}$
ii) $(721)_{8}-(32)_{8}$
iii) BCD addition of 01100111 and 01010011

2 Perform the following conversions: (Show the steps of conversion)
i) $(463.25)_{10}$ to binary
ii) $(36.25)_{10}$ to octal
iii) (AF9.0C) ${ }_{16}$ to binary

3 Using Boolean postulates simplify the following expressions:
i) $x+x$ ' $y$
ii) $x y+x$ 'z $+y z$
iii) $x^{\prime} y^{\prime} z+x^{\prime} y z+x y$ '

4 Express the following functions:
i) $F_{1}=A B+B^{\prime} C$ in sum of Minterms form.
ii) $\mathrm{F}_{2}=\mathrm{A}+\mathrm{B}^{\prime} \mathrm{C}$ in product of Maxterms form.

PART B
Answer any two full questions, each carries 9 marks
5 Perform subtraction of the following using r's complement and (r-1)'s complement methods:
i) $(7235)_{10-}(346)_{10}$
ii) $(1000100)_{2^{-}}(1110100)_{2}$

Given $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum(1,4,6,7,8,9,10,11,15)$. Simplify using Quin-
McClusky method and determine the prime implicants, essential prime implicants and the minimized Boolean expression.
7 a) Using K-map, simplify the Boolean function F in sum of products form, using the don't care conditions d:
$F(w, x, y, z)=w^{\prime}\left(x^{\prime} y+x^{\prime} y^{\prime}+x y z\right)+x^{\prime} z^{\prime}(y+w)$
$d(w, x, y, z)=w^{\prime} x\left(y^{\prime} z+y z '\right)+w y z$
b) Give the IEEE Single precision format for floating point number representation with explanation. Determine the floating-point binary number represented by the following single precision floating point representation.
"1100 $1010110001110001000000111011 "$

## PART C <br> Answer all questions, each carries 3 marks

8 Implement $\mathrm{F}=\mathrm{A}(\mathrm{B}+\mathrm{CD})+\mathrm{B}^{\prime} \mathrm{C}$ with NAND gates.
9 Derive the simplified Boolean output functions of a full subtractor.
10 Explain the terms:
i) Race-around condition
ii) Edge triggering of flip-flops

11 Implement D flip- flop using NAND gates and explain its working.

## PART D <br> Answer any two full questions, each carries 9 marks

12 a) Implement a 4- bit magnitude comparator. Give a Boolean function to check the equality relation of a pair of bits and derive logic functions for the outputs of the magnitude comparator.
b) Give the characteristic table and excitation table of RS flip-flop and JK flip flop.
a) Implement the function with a multiplexer: $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum(0,1,3,4,8,9,15)$
b) Explain state table and state diagram with an example.
a) What is a Master-slave flip-flop? Explain its working with a timing diagram.
b) How can the principle of look- ahead carry reduce the carry propagation time in a binary parallel adder? Derive the Boolean functions for the carry outputs at different stages of a look-ahead carry generator.

## PART E

Answer any four full questions, each carries 10 marks
15 Design a BCD ripple counter. Also verify its operation by means of a timing diagram.
a) Explain PLA with a block diagram.
b) Design a counter that has a repeated sequence of the following six states: 000, $001,010,100,101,110$
17 a) Explain the various types of ROMs
b) Implement a 4- bit bidirectional shift register with parallel load.

18 a) Sketch the block diagram of a BCD adder. Using a truth table derive the condition for correction in BCD addition.
b) Design a serial adder using a full adder and shift registers.
a) Explain the construction of a 32 X 4 ROM with a logic diagram.
b) Give the logical configuration of shift registers. With a block diagram, explain the use of shift registers for serial transfer of data. Draw a flow chart and explain the addition/ subtraction of two binary numbers in signed magnitude representation.

